WHAT IS CLAIMED IS:

1. A method of simulating a memory circuit design in order to verify the signal strength of bit lines, the method comprising the steps of:

identifying circuit elements of the memory circuit design;

extracting a memory circuit path from the circuit elements;

simulating the memory circuit;

measuring a maximum voltage difference between bit lines; and

comparing the maximum voltage difference between bit lines to a noise margin to verify the signal strength of the bit lines.

2. The method of claim 1 wherein the voltage difference between bit lines is the voltage difference between bit and bitb lines.

3. The method of claim 1 further comprising the step of identifying sense amplifier enable node after extracting the memory circuit path.

4. The method of claim 3 further comprising the step of measuring the voltage difference between bit lines at a sensing time controlled by the sense amplifier enable node.

5. The method of claim 4 further comprising the step of comparing the voltage difference between bit lines to a noise margin at the sensing time to verify the signal strength of the bit lines.

6. The method of claim 5 wherein the voltage difference between bit lines is the voltage difference between bit and bitb lines.

7. A system for simulating a memory circuit design in order to verify the signal strength of bit lines, the system comprising:

a computer configured to execute the following instructions:

identify circuit elements of the memory circuit design;

extract a memory circuit path from the circuit elements;

simulate the memory circuit;

measure a maximum voltage difference between bit lines; and

compare the maximum voltage difference between bit lines to a noise margin to verify the signal strength of the bit lines.

8. The system of claim 7 wherein the voltage difference between bit lines is the voltage difference between bit and bitb lines.

9. The system of claim 7 wherein the computer is further configured to identify a sense amplifier enable node after extracting the memory circuit path.

10. The system of claim 9 wherein the computer is configured to measure the voltage difference between bit lines at a sensing time controlled by the sense amplifier enable node.

11. The system of claim 10 wherein the computer is configured to compare the voltage difference between bit lines to a noise margin at the sensing time to verify the signal strength of the bit lines.

12. The system of claim 11 wherein the voltage difference between bit lines is the voltage difference between bit and bitb lines.

13. A method of characterizing a minimum clock cycle time against a noise margin in a memory circuit design, the method comprising the steps:

identifying circuit elements of the memory circuit design;

extracting a memory circuit path from the circuit elements;

simulating the memory circuit with a maximum initial clock cycle time;

simulating the memory circuit with a minimum initial clock cycle time;

calculating the criterion parameter for the simulations; and

determining whether the simulations are successful to determine if the minimum clock cycle time is valid.

14. The method of claim 13 further comprising the steps;

determining a new clock cycle time if the simulations are not successful;

simulating the memory circuit with the new clock cycle time; and

determining whether the simulations are successful to determine if the minimum clock cycle time is valid.

15. The method of claim 14 comprising the steps of repeatedly determining a new clock cycle time, simulating the memory circuit with the new clock cycle time and determining whether the simulations are successful until the criterion parameter converges to a prescribed value.

16. The method of claim 14 wherein the simulations are not successful if a data output error of the simulation is above a prescribed value.

17. The method of claim 14 wherein the simulations are not successful if a voltage difference between bit and bitb lines of the memory circuit is less than the prescribed noise margin.

18. A system for characterizing a minimum clock cycle time against a noise margin in a memory circuit design, the system comprising:

a computer configured to execute the following procedure:

identify circuit elements of the memory circuit design;

extract a memory circuit path from the circuit elements;

simulate the memory circuit with a maximum initial clock cycle time;

simulate the memory circuit with a minimum initial clock cycle time;

calculate a criterion parameter for the simulations; and

determine whether the simulations are successful to determine if the minimum clock cycle time is valid.

19. The system of claim 18 wherein the computer is configured to further execute the following procedure;

determine a new clock cycle time if the simulations are not successful;

simulate the memory circuit with the new clock cycle time; and

determine whether the simulations are successful to determine if the minimum clock cycle time is valid.

20. The system of claim 19 wherein the computer is configured to repeatedly determine a new clock cycle time, simulate the memory circuit with the new clock cycle time and determine whether the simulations are successful until the criterion parameter converges to a prescribed value.

21. The system of claim 20 wherein the simulations are not successful if a data output error of the simulation is above a prescribed value.

22. The method of claim 20 wherein the simulations are not successful if a voltage difference between bit and bitb lines of the memory circuit is less than the prescribed noise margin.

23. A method of characterizing a minimum circuit parameter sensitive to a noise disturbance against a noise margin in a circuit design, the method comprising the steps:

identifying circuit elements to be characterized;

extracting a critical path netlist from the circuit elements;

simulating the critical path netlist with a maximum initial value of the parameter under characterization;

simulating the critical path netlist with a minimum initial value of the parameter under characterization;

calculating a criterion parameter;

determining whether the simulations based on the initial minimum and maximum values of the parameter under characterization indicate the same status; and

ceasing simulation if both simulations indicate the same status.

24. The method of claim 23 further comprising the steps:

determining a current value of the parameter under characterization that is half the sum of the maximum initial and minimum initial values of the parameter;

simulating the critical path netlist with the current value of the parameter and determining against the noise margin whether the simulation indicates a success or failed status;

setting the current value of the parameter to the current minimum value of the parameter if both simulations based on the two values of the parameter indicate the same status; and

setting the current value of the parameter to the current maximum value of the parameter otherwise.

25. The method of claim 24 comprising the steps of repeatedly determining a new current value of the parameter under characterization, simulating the critical path netlist with the new value of the parameter and determining against the noise margin whether the simulations indicate a success or failed status until the criterion parameter converges to a prescribed bisection.

26. The method of claim 24 wherein the simulation indicates a success or failed status if a data output error of the simulation is above a prescribed threshold.

27. The method of claim 24 wherein the simulation indicates a failed status if the measured noise is above the prescribed noise margin.

28. A system for characterizing a minimum value of circuit parameter against a noise margin, the system comprising:

a computer configured to execute the following procedure:

identify circuit elements of the circuit to be characterized;

extract a critical path netlist from the circuit elements;

simulate the critical path netlist with a maximum initial value of the parameter under characterization;

simulate the critical path netlist with a minimum initial value of the parameter under characterization;

calculate a criterion parameter;

determine whether the simulations based on the initial minimum and maximum values of the parameter indicate the same status; and

halt operations if both simulations indicate the same status.

29. The system of claim 28 wherein the computer is configured to further execute the following procedure:

determine a current value of the parameter that is half the sum of the maximum initial and minimum initial values of the parameter;

simulate the critical path netlist with the current value of the parameter and determine against the noise margin whether the simulation indicates a success or failed status;

set the current value of the parameter to the current minimum value of the parameter if both simulations based on the two values of the parameter indicate the same status; and

set the current value of the parameter to the current minimum value of the parameter otherwise.

30. The system of claim 29 wherein the computer is configured to repeatedly determine a new value of the parameter under characterization, simulate the critical path netlist with the new value of the parameter and determine against the noise margin whether the simulation indicates a success or failed status until the criterion parameter converges to a prescribed value.

31. The system of claim 30 wherein the simulation indicates a failed status if a data output error of the simulation is above a prescribed threshold value.

32. The system of claim 30 wherein the simulation indicates a failed status if measured noise is above the prescribed noise margin.

33. A method of simulating and determining an optimized circuit parameter simultaneously, the method comprising the following steps:

defining a circuit path of the circuit;

simulating the circuit path with the parameter under characterization; and

determining whether the parameter under characterization is optimized with the circuit simulation.

34. The method of claim 33 wherein the circuit is simulated with a new parameter under characterization until the parameter under characterization is optimized.

35. The method of claim 33 wherein the parameter under characterization is optimized when a bisection error of the circuit simulation is within a prescribed range.

36. The method of claim 35 wherein the parameter under characterization is a signal strength of a prescribed signal.